Integration Film Scheme for Copper / Low-k Interconnect

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application relates to the following co-pending and commonly assigned patent application: Serial No. 10/602,751, filed on June 24, 2003, entitled Hybrid Copper / Low k Dielectric Interconnect Integration Method and Device, which application is hereby incorporated herein by reference.

TECHNICAL FIELD

[0002] The present invention relates generally semiconductor devices, and more particularly to semiconductor devices having multiple layers of metallization.

BACKGROUND

[0003] As semiconductor device circuit density increases and device feature size decreases, increased numbers of patterned metal levels are required with decreased spacing between metal lines at each level to effectively interconnect discrete semiconductor devices on semiconductor chips. The different levels of metal interconnections are separated by layers of insulating materials or films, often referred to as inter-level dielectric (ILD) layers. These interposed insulating layers have etched holes or trenches that are filled with a conductive material, referred to as vias or plugs, which are used to connect one level of metallization lines to the next. A common insulating material used for ILD layers is silicon oxide (SiO_2), which has a dielectric constant (k) of about 4.0 to 4.5, relative to a vacuum, which has a k value of 1.0.

[0004] However, as semiconductor device dimensions decrease and the packing density increases, it is necessary to reduce the spacing between the metal lines at each level of

interconnection to wire up the integrated circuits. Unfortunately, as the spacing decreases, the intra-level and inter-level capacitances increase between metal lines, as capacitance is inversely proportional to the spacing between the lines. Therefore, it is desirable to minimize the dielectric constant k of the insulating material (dielectric) between the conducting lines, in order to reduce the RC time constant and thereby increase the performance of the circuit, e.g., the frequency response, since the signal propagation time in the circuit is adversely affected by the RC delay time.

[0005] To achieve an insulating layer with a dielectric constant of 3 or less, low-k insulating films are often used for ILD layers. However, lower-k dielectric materials usually have poor mechanical strength and related properties. In general, the lower the k value, the poorer the mechanical strength. Introducing low-k insulating materials into a multi-level metallization integration scheme results in a mechanically weak and vulnerable low-k interconnect stack, degrading the reliability of the semiconductor device and resulting in device failures.

SUMMARY OF THE INVENTION

[0006] These and other problems are generally solved or circumvented, and technical advantages are generally achieved, by preferred embodiments of the present invention, which provide a novel integration scheme for multi-layer metallization using low-dielectric constant materials. A single ILD layer includes three or more sub-layers of low-dielectric constant material, wherein adjacent sub-layers have different properties. The single ILD layer may comprise one type of low-dielectric constant material, wherein parameters are changed during deposition to achieve the different properties of the three or more sub-layers of low-dielectric constant material. Adjacent sub-layers of the ILD layer may have different dielectric constants, densities, Young's modulus, and adhesion properties, as examples.

[0007] In accordance with a preferred embodiment of the present invention, a method of manufacturing an inter-level dielectric (ILD) layer of a semiconductor device includes forming a first low-dielectric constant material sub-layer over the substrate, the first low-dielectric constant material having at least one first material property, and forming a second low-dielectric constant material sub-layer over the first low-dielectric constant material sub-layer, the second low-dielectric constant material sub-layer having at least one second material property, wherein the at least one second material property is different from the at least one first material property. The method includes forming a third low-dielectric constant material sub-layer over the second low-dielectric constant material sub-layer, the third low-dielectric constant material sub-layer having at least one third material property, the at least one third material property being different from the at least one second material property.

[0008] In accordance with another preferred embodiment of the present invention, a method of manufacturing a semiconductor device includes providing a substrate, the substrate having component regions formed thereon, forming a first etch stop layer over the substrate, and forming a first ILD layer over the first etch stop layer. At least one first conductive region is formed in the first ILD layer and first etch stop layer, wherein at least one first conductive region makes electrical contact with at least one component region of the substrate. Forming the first ILD layer comprises forming a first low-dielectric constant material sub-layer over the first etch stop layer, and forming a second low-dielectric constant material sub-layer over the first low-dielectric constant material sub-layer, the second low-dielectric constant material sub-layer having at least one different material property than the first low-dielectric constant material sub-layer. Forming the ILD layer includes forming a third low-dielectric constant material sub-layer over the second low-dielectric constant material sub-layer, the third low-dielectric constant material sub-layer having at least one different material property than the second low-dielectric constant material sub-layer.

[0009] In accordance with yet another preferred embodiment of the present invention, an ILD layer of a semiconductor device includes a first low-dielectric constant material sub-layer, the first low-dielectric constant material having at least one first material property, and a second low-dielectric constant material sub-layer disposed over the first low-dielectric constant material sub-layer, the second low-dielectric constant material sub-layer having at least one second material property, wherein the at least one second material property is different from the at least one first material property. The ILD layer includes a third low-dielectric constant material sub-layer disposed over the second low-dielectric constant material sub-layer, the third low-dielectric

constant material sub-layer having at least one third material property, the at least one third material property being different from the at least one second material property.

[0010] In accordance with another preferred embodiment of the present invention, a semiconductor device includes a substrate, the substrate having component regions formed thereon, a first etch stop layer disposed over the substrate, and a first ILD layer disposed over the first etch stop layer. At least one first conductive region is formed in the first ILD layer and first etch stop layer, wherein at least one first conductive region makes electrical contact with at least one component region of the substrate. The first ILD layer includes a first low-dielectric constant material sub-layer disposed over the first etch stop layer, and a second low-dielectric constant material sub-layer disposed over the first low-dielectric constant material sub-layer, the second low-dielectric constant material sub-layer having at least one different material property than the first low-dielectric constant material sub-layer. A third low-dielectric constant material sub-layer is disposed over the second low-dielectric constant material sub-layer, the third low-dielectric constant material sub-layer having at least one different material property than the second low-dielectric constant material sub-layer.

[0011] Advantages of preferred embodiments of the present invention include providing a multi-layer metallization structure and method of manufacturing thereof wherein the ILD layers comprise low-dielectric constant materials, yet have increased mechanical strength. Semiconductor devices utilizing the novel metallization ILD scheme described herein have improved reliability and increased yields.

[0012] The foregoing has outlined rather broadly the features and technical advantages of embodiments of the present invention in order that the detailed description of the invention that follows may be better understood. Additional features and advantages of embodiments of the

invention will be described hereinafter, which form the subject of the claims of the invention. It should be appreciated by those skilled in the art that the conception and specific embodiments disclosed may be readily utilized as a basis for modifying or designing other structures or processes for carrying out the same purposes of the present invention. It should also be realized by those skilled in the art that such equivalent constructions do not depart from the spirit and scope of the invention as set forth in the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] For a more complete understanding of embodiments of the present invention and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

[0014] Figure 1 shows a cross-sectional view of an ILD layer having three or more sub-layers in accordance with an embodiment of the present invention;

[0015] Figure 2 shows another cross-sectional view of an ILD layer in accordance with a preferred embodiment of the invention;

[0016] Figure 3 illustrates a cross-sectional view of a semiconductor device having many ILD layers manufactured in accordance with a preferred embodiment of the present invention; and

[0017] Figures 4A through 4C show alternative embodiments of the present invention in a cross-sectional view.

[0018] Corresponding numerals and symbols in the different figures generally refer to corresponding parts unless otherwise indicated. The figures are drawn to clearly illustrate the relevant aspects of the preferred embodiments and are not necessarily drawn to scale.

DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

[0019] The making and using of the presently preferred embodiments are discussed in detail below. It should be appreciated, however, that the present invention provides many applicable inventive concepts that can be embodied in a wide variety of specific contexts. The specific embodiments discussed are merely illustrative of specific ways to make and use the invention, and do not limit the scope of the invention.

[0020] With reference to Figure 1, a cross-sectional view of an ILD layer 102 manufactured in accordance with a preferred embodiment of the present invention is shown. The ILD layer 102 includes an etch stop layer (ESL) 104. The etch stop layer 104 may comprise SiC, SiCO, SiCN, combinations thereof, or other insulating materials, as examples, deposited using CVD or PECVD to a thickness of 200 to 1,000 Angstroms, as examples. The etch stop layer 104 protects an underlying insulating layer (not shown in Figure 1; see Figure 3) during the patterning or etching of the ILD layer 102, and also provides improved adhesion for subsequently formed low-dielectric constant material sub-layers 106, 108 and 112.

[0021] The ILD layer 102 includes three or more low-dielectric constant material sub-layers 106, 108, and 112 in accordance with an embodiment of the present invention. The ILD layer 102 includes a first low-dielectric constant material sub-layer 106 disposed over the etch stop layer 104. A second low-dielectric constant material sub-layer 108 is disposed over the first low-dielectric constant material sub-layer 106, and at least a third low-dielectric constant material sub-layer 112 is disposed over the second low-dielectric constant material sub-layer 108. The ILD layer 102 may include additional low-dielectric constant material sub-layers, not shown.

[0022] An etch stop layer 114 may be deposited over the ILD layer 102. The top etch stop layer 114 protects the ILD layer 102 during etch processes and improves adhesion of subsequently-deposited ILD layers, not shown (see Figure 3). The etch stop layer 114 may be deposited either before or after the patterning of the ILD layer 102.

[0023] Contact openings may be formed in the etch stop layer 114 and ILD 102 and may be filled with a conductive material (not shown in Figure 1; see Figure 3). The contact opening may be filled with a conductive plug comprising tungsten, aluminum, doped polysilicon, or some other appropriate conductive material. The plug may include adhesion and barrier layers, such as titanium and titanium nitride, respectively, for improved device characteristics. Alternatively, a single or dual damascene process may be employed to form trenches and holes in the ILD layer 102 for conductive lines and/or vias, followed by filling, growing or depositing a conductive material such as copper within the trenches and holes to form the conductive lines and vias.

[0024] Preferably, each low-dielectric constant material sub-layer 106, 108, and 112 has at least one different material property than an adjacent low-dielectric constant material sub-layer 106, 108, and 112. For example, they may have different low-dielectric constants (k) and/or densities and may comprise different low-k materials altogether. In one embodiment, the lowest level low-dielectric constant material sub-layer 106 (the sub-layer adjacent the bottom etch stop layer 104) comprises a lower dielectric constant k than the dielectric constant of the other upper sub-layers 108 and 112. For example, first low-dielectric constant material sub-layer 106 may comprise a dielectric constant of below about 2.8, e.g., ranging from about 2.2 to 2.5, and the second low-dielectric constant material 108 and third low-dielectric constant material 112 may comprise dielectric constants of about 2.8 or greater, e.g., about 2.8 to 3.3. As another example, the first low-dielectric constant material sub-layer 106 may comprise a density of about 0.89 to

1.2, and the second low-dielectric constant material sub-layer 108 and third low-dielectric constant material sub-layer 108 may comprise a density of between about 1.2 to 1.8.

[0025] In another embodiment, the Young's modulus of the first low-dielectric constant material sub-layer 106 may be smaller than the Young's modulus of the second and third low-dielectric constant materials 108 and 112. For example, the Young's modulus of the first low-dielectric constant material sub-layer 106 may be about 20 GPa and the Young's modulus of the second and third low-dielectric constant materials 108 and 112 may be about 10 GPa or smaller. As another example, the first low-dielectric constant material sub-layer 106 may have a Young's modulus of about 10 GPa or less, the second low-dielectric constant material 108 may have a Young's modulus of about 10-15 GPa, and the third low-dielectric constant material 112 may have a Young's modulus of about 5-10 GPa.

[0026] In yet another embodiment, the first low-dielectric constant material sub-layer 106 may be more adhesive than the second and third low-dielectric constant materials 108 and 112, for example. This is advantageous in that adhesion of the first low-dielectric constant material sub-layer 106 to the etch stop layer 104 is improved. The adhesion of the first low-dielectric constant material sub-layer 106 may be greater than about 10 J/m^2, and the adhesion of the second and third low-dielectric constant materials 108 and 112 may be less than about 10 J/m^2, as examples.

[0027] In one embodiment, the low-k material sub-layers 106, 108 and 112 preferably comprise only one single type of material, wherein the deposition conditions are changed or adjusted during a continuous deposition process in one or more deposition chambers while the single type of material is deposited. The changes in the deposition conditions create the different material properties of the low-dielectric material sub-layers 106, 108, and 112. For example,

parameters of the deposition process that may be changed include the gas flow rate, power level, or gas species, as examples. Alternatively, other deposition process parameters that may be changed or adjusted to create the different material properties of the low-dielectric constant material sub-layers 106, 108, and 112 include temperature and pressure, as examples. In another embodiment, each low-dielectric material sub-layer 106, 108, and 112 may comprise a different type of low-k material, for example.

[0028] The low-k material sub-layers 106, 108, and 112 preferably comprise low-dielectric constant materials such as methyl silsesquioxane (MSQ), a MSQ derivative, hydridosilsesquioxane (HSQ), a HSQ derivative, an oxide and MSQ hybrid, a porogen/MSQ hybrid, an oxide and HSQ hybrid, a porogen/HSQ hybrid, or combinations thereof, as examples. Alternatively, the low-k material sub-layers 106, 108, and 112 may comprise other low-dielectric constant materials, such as nanoporous silica, xerogel, polytetrafluoroethylene (PTFE), or low-dielectric constant (low-k) materials such as SiLK available from Dow Chemicals of Midland, Michigan, Flare, available from Allied Signal of Morristown, New Jersey, and Black Diamond, available from Applied Materials of Santa Clara, California, as examples, although other low-k materials may also be used. The sub-layers 106, 108, and 112 are preferably deposited using a chemical vapor deposition ("CVD") or a spin-on coating technique, although other deposition techniques may alternatively be used. The ILD layer 102 is preferably deposited to a thickness of approximately 2,000 to 9,000 Angstroms, for example, although the ILD layer 102 may comprise other thicknesses. One skilled in the art will recognize that the preferred thickness range will be a matter of design choice and will likely decrease as device critical dimensions shrink and processing controls improve over time.

[0029] In a preferred embodiment of the present invention, preferably, the first, second and third low-dielectric constant material sub-layers 106, 108, and 112 comprise low-dielectric MSQ, for example. A substrate (not shown in Figure 1; see Figure 3) is placed in a deposition chamber. Deposition chemistries are introduced into the deposition chamber at a first temperature and a first gas flow rate for a period of time to form the first low-dielectric constant material sub-layer 106 having a dielectric constant of about 2.5 and a density of 0.9, as an example. The gas flow rate is changed to a second gas flow rate to form the second low-dielectric constant material sub-layer 108 having a dielectric constant of about 3.0 and a density of about 1.5. The gas flow rate is changed to a third gas flow rate to form the third low-dielectric constant material sub-layer 112 having a dielectric constant of about 3.3 and a density of about 1.7. Alternatively, to achieve the different material properties of the sub-layers 106, 108, and 112, other deposition process parameters may be adjusted, such as the power level, gas species introduced to the deposition chamber, temperature, and/or pressure, or combinations of the various process parameters described herein, as examples.

[0030] Figure 2 shows another cross-sectional view of an ILD layer 202 in accordance with another preferred embodiment of the invention. The ILD layer 202 includes an etch stop layer 204 comprising SiC, SiCO, SiCN, combinations thereof, or other insulating materials, as examples, deposited using CVD or PECVD to a thickness of 200 to 1,000 Angstroms, as examples. The low-dielectric constant material sub-layers 206, 208, 212, and 216 are numbered sequentially: low-dielectric constant material sub-layer 206 is deposited first, indicated by the number 1 in Figure 2. A first low-dielectric constant material sub-layer 206 is formed over the etch stop layer 204. One or more parameters of the deposition process is modified or adjusted to form a second low-dielectric constant material sub-layer 208 (layer number 2) disposed over and

abutting the first low-dielectric constant material sub-layer 206. The second low-dielectric constant material sub-layer 208 may comprise the same material having one or more different material parameters, such as density, dielectric constant, adhesion, and Young's modulus, as examples, than the first low-dielectric constant material sub-layer 206 in one embodiment. Alternatively, the second low-dielectric constant material sub-layer 208 may comprise a different material than the first low-dielectric constant material sub-layer 206.

[0031] One or more parameters of the deposition process is modified or adjusted to form a third low-dielectric constant material sub-layer 212 (layer number (n-1)) disposed over and abutting the second low-dielectric constant material sub-layer 208. The third low-dielectric constant material sub-layer 212 comprises the same material having at least one different parameter, such as density, dielectric constant, adhesion, and Young's modulus, as examples, than the second low-dielectric constant material sub-layer 208 in one embodiment. Alternatively, the third low-dielectric constant material sub-layer 212 may comprise a different material than the second low-dielectric constant material sub-layer 208.

[0032] One or more parameters of the deposition process is modified or adjusted to form a fourth low-dielectric constant material sub-layer 216 (layer number n) over and abutting the third low-dielectric constant material sub-layer 212. The fourth low-dielectric constant material sub-layer 216 comprises the same material having at least one different parameter, such as density, dielectric constant, adhesion, and Young's modulus, as examples, than the third low-dielectric constant material sub-layer 212 in one embodiment. Alternatively, the fourth low-dielectric constant material sub-layer 216 may comprise a different material than the third low-dielectric constant material sub-layer 212.

[0033] The total number of sub-layers n of the ILD layer 202 preferably comprises three or more, and may comprise five or more in one embodiment, for example. An etch stop layer 214 may be deposited over the top low dielectric constant material 216, before or after patterning the ILD layer 202, as shown.

[0034] Figure 3 illustrates a cross-sectional view of a semiconductor device 300 having many ILD layers 302 (shown as 302a through 302g), as described herein with reference to ILD layer 102 of Fig. 1 and ILD layer 202 of Figure 2, manufactured in accordance with a preferred embodiment of the present invention. Figure 3 illustrates a portion of an integrated circuit embodying aspects of the present invention. In particular, device 300 includes a substrate 320 comprising a single semiconductor wafer, such as a single crystal silicon wafer. Alternatively, the substrate 300 may comprise a thin silicon layer formed over a buried oxide, such as a silicon-on-insulator (SOI) substrate, or other semiconductor materials, as examples. A component region 322 is formed in the substrate 300. The component region 322 may comprise a first transistor and a second transistor, separated by an isolation region, as shown, although the component region 322 may alternatively comprise other elements or circuits, for example. There may be many component regions 322 formed in the substrate (not shown). The details regarding the formation of the component regions 322 are omitted because they are not necessary for an understanding of the invention.

[0035] The semiconductor device 300 includes a stack of ten or more metallization layers disposed over the component region 322, as shown. The metallization layers connect the component region 322 to other transistors and devices (not shown) on the integrated circuit, including ground nodes and voltage nodes. The metallization layers also connect the various

component regions 322 of the integrated circuit to circuitry, signals, and voltages external to the integrated circuit device.

[0036] A dielectric layer 324 overlies and electrically insulates the component regions 322 formed within or on the substrate 320 from subsequently formed layers, such as metal layer 332. Electrical contact to the component regions 322 formed within or on the substrate 320 is accomplished by way of contacts 326 through an etch stop layer 328 and dielectric layer 324. In the illustrated embodiment, only one contact is shown connecting to a doped region of a transistor of the component region 322, for clarity. One skilled in the art will recognize that multiple contacts may be made to the component regions 322, including connection to other doped regions and to the gates of the component region 322, although these have been omitted from the drawings for clarity. A first metal pattern 332 is formed above the component region 322 and is electrically coupled to the component region 322 via contacts 326. This first metal pattern 332 is electrically insulated from other conductive components by dielectric layer 330, etch stop layer 328, and by dielectric layer 324. The dielectric layers 330 and 324 may comprise silicon dioxide, undoped silicon glass (USG) or low-k materials, for example.

[0037] An etch stop layer 304a is deposited over the dielectric layer 330, as described herein with reference to etch stop layer 104 in Figure 1 and 204 in Figure 2. Three or more low-dielectric constant material sub-layers 306a, 308a, and 312a are formed sequentially over the etch stop layer 304a, as shown, also as described with reference to low-dielectric constant material sub-layers 106, 108, and 112 in Figure 1 and low-dielectric constant material sub-layers 206, 208, and 212 in Figure 2. Adjacent low-dielectric constant material sub-layers 306a and 308a preferably comprise at least one material property difference. Similarly, adjacent low-dielectric constant material sub-layers 308a and 312a preferably comprise at least one material

property difference. The sub-layers 306a, 308a, and 312a preferably comprise the same material deposited continuously in one or more deposition chambers, in one embodiment.

[0038] The low-k material sub-layers 306a, 308a, and 312a are patterned using lithography techniques with a pattern for the desired metallization layers and vias. For example, in a dual damascene process, vias 346a may be patterned, followed by the patterning of conductive lines 348a. Alternatively, the conductive lines 348a may be patterned before the vias 346a are patterned. The plurality of low-k material sub-layers 306a, 308a, and 312a are preferably patterned as a single layer. A conductive material such as copper is deposited over the patterned low-k material sub-layers 306a, 308a, and 312a, and excess conductive material is removed from the top surface of the top low-k material sub-layer 312a, using a chemical-mechanical polish (CMP) process, for example, forming conductive lines 348a and vias 346a that make electrical contact to conductive line 332, as shown. Conductive lines 348a and vias 346a form a single metallization layer of the semiconductor device 300. Barrier liners and seed layers may be deposited before filling the patterned low-k material sub-layers 306a, 308a, and 312a with conductive material, for example, not shown.

[0039] The process is repeated to form a plurality of additional metallization layers, as described herein and with reference to ILD layers 302b, 302c, 302d, 302e, 302f, and 302g and etch stop layers 304c, 304d, 304e, 304f, and 304g. While seven layers of ILD layers are shown in Figure 3, there may be more, or fewer ILD layers formed from three or more low-k material sub-layers 306, 308, and 312 (shown in Figure 3 as 306a-306g, 308a-308g, and 312a-312g) on the semiconductor device 300.

[0040] Note that the etch stop layer 304b may be deposited over the top low-k material sub-layer 312a either prior to, or after, the patterning of the low-k material sub-layers 312a, 308a, and

306a. If the etch stop layer 304b is deposited over the low-k material sub-layer 312 prior to the patterning of the low-k material sub-layers 312a, 308a, and 306a, the etch stop layer 304b must be patterned in addition to the patterning of the low-k material sub-layers 312a, 308a, and 306a so that electrical contact will be made from vias 346a-346g to 332 and 348a-348f, respectively. The etch stop layer 304b protects the top low-dielectric constant material sub-layer 312a during the CMP process to remove excess conductive material.

[0041] Processing of the semiconductor device 300 is then continued to complete the device. For example, an etch stop layer 314a may be deposited over the top ILD layer 302g, and a dielectric layer 334a may be deposited over the etch stop layer 314a. The dielectric layer 334a may be patterned with a via to connect to conductive line 348g, and a conductive material may be deposited to fill the via pattern. Another etch stop layer 336a may be deposited over the dielectric layer 334a, and another dielectric layer 338a may be deposited over the etch stop layer 336a. Conductive lines 350a may be formed in the dielectric layer 338a and etch stop layer 336a by patterning the dielectric layer 338a and etch stop layer 336a and depositing a conductive material. Additional dielectric layers 334b and 338b and etch stop layers 314b and 336b may be similarly deposited, patterned and filled to form vias and conductive lines 350b in single damascene processes, as required. Additional etch stop layer 340 and insulating layers 342 and 344 may be deposited over the dielectric layer 338b and conductive lines 350b, as shown.

[0042] Dielectric layers 334a, 338a, 334b, and 338b (being the top several dielectric layers in which are formed metal patterns 350a and 350b, respectively) are preferably formed of a material having a dielectric constant in the range of about 3.0 to 4.2, in one embodiment. One exemplary such material is undoped silicon glass (USG) that may be spun onto the substrate surface and subsequently patterned. In other instances, FSG or other well-known alternatives,

having acceptably low-k characteristics, may alternatively be used. While the layer thickness is a matter of design choice and process control, the upper layers are preferably deposited to a thickness in the range of from about 6,000 to 15,000 Angstroms.

[0043] Figures 4A through 4C show cross-sectional views of alternative embodiments of the present invention. In one embodiment, vias 346a are formed in the first low-k material sub-layer 306a and the etch stop layer 304a, and conductive lines 348a are formed in the second low-k material sub-layer 308a and the third low-k material sub-layer 312a, as shown in Figures 3 and 4A. In another embodiment, vias 446 are formed in an etch stop layer 404, a first low-k material sub-layer 406, and a second low-k material sub-layer 408, and conductive lines 448 are formed in a third low-k material sub-layer 412, as shown in Figure 4B. In yet another embodiment, vias 546 are formed in an etch stop layer 504, a first low-k material sub-layer 506, a second low-k material sub-layer 508, a third low-k material sub-layer 512a, and a fourth low-k material sub-layer 512b, and conductive lines 548 are formed in a fifth low-k material sub-layer 512c and a sixth low-k material sub-layer 512d, as shown in Figure 4C. Similarly, vias may be formed in one or more low-k material sub-layers, and conductive lines may be formed in one or more low-k material sub-layers in accordance with embodiments of the present invention.

[0044] Advantages of embodiments of the invention include providing a novel multi-level interconnect scheme for semiconductor devices that provides a low-dielectric constant ILD layer with optimum material properties to reduce the RC time delay in multi-level metallization structures. More robust multi-level inter-connect layers result from the method of manufacturing described herein, having improved structural strength. Embodiments of the present invention result in increased yields and improved reliability.

[0045] Although embodiments of the present invention and their advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the spirit and scope of the invention as defined by the appended claims. For example, it will be readily understood by those skilled in the art that many of the features, functions, processes, and materials described herein may be varied while remaining within the scope of the present invention. Moreover, the scope of the present application is not intended to be limited to the particular embodiments of the process, machine, manufacture, composition of matter, means, methods and steps described in the specification. As one of ordinary skill in the art will readily appreciate from the disclosure of the present invention, processes, machines, manufacture, compositions of matter, means, methods, or steps, presently existing or later to be developed, that perform substantially the same function or achieve substantially the same result as the corresponding embodiments described herein may be utilized according to the present invention. Accordingly, the appended claims are intended to include within their scope such processes, machines, manufacture, compositions of matter, means, methods, or steps.